1. Which one is the characteristic of Harvard Architecture?
2. Program and Data stored in Separate Memory
3. Program and Data stored in same Memory
4. Program and data stored in Cache Memory
5. All of Above
6. Which of the following is the working cycle of CPU?
7. Decode, Execute, Fetch
8. Fetch, Decode, Execute
9. Fetch, Execute, Decode
10. All of Above
11. Any condition that causes a processor to stall is called as \_\_\_\_\_\_\_\_\_
12. Hazard
13. Page fault
14. System error
15. None of the mentioned
16. What does the control unit generate to control other units?
    1. Transfer signals
    2. Command Signal
    3. Control signals
    4. Timing signals
17. What do the processors of all computers must have?
    1. Control unit
    2. ALU
    3. Register
    4. All of these
18. Which is the fastest memory in the computer?
19. Cache
20. RAM
21. Register
22. Hard disk
23. With the help of \_\_\_\_\_\_\_ we reduce the memory access time:
    1. SDRAM
    2. Cache
    3. Heaps
    4. Higher capacity RAMs
24. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution?
    1. ISA
    2. ANSA
    3. Super-scalar
    4. All of the mentioned
25. A processor performing fetch or decoding of different instruction during the execution of another instruction is called \_\_\_\_\_\_
    1. Super-scaling
    2. Pipe-lining
    3. Parallel Computation
    4. None of the mentioned
26. A 24-bit address generates an address space of \_\_\_\_\_\_ locations.
    1. 1024
    2. 4096
    3. 248
    4. 16,777,216
27. The USA contains about 3100 counties. Suppose you have a table that stores, for each county, its name (up to 40 characters in 8-bit ASCII), its state (a two-letter code), its population, and its median income (both as 32-bit numbers). How much space would the whole database take in memory?

**Name** = 40 Characters = 40 bytes

**State** = 2 Characters = 2 bytes

**Population** = 32-bit integer = 4 bytes

**Median income** = 32-bit integer = 4 bytes

Hence, **Total number of bytes** = 40 + 2 + 4 + 4 = 50 bytes

Therefore, for 31 rows, the table = 3100 \* 50 = 155,000 bytes

or, 155,000 bytes = 151KB approx.

1. The computer has a maximum addressable memory of 16 Gigabytes. Its address bus width is 32.
2. Calculate the width of the data bus.

Width of the data bus = 232 = 4294967296 bytes = 4 GB

1. State the effect that adding one new line to the address bus would have on the maximum addressable memory.

232 = 4 GB

233 = 8 GB

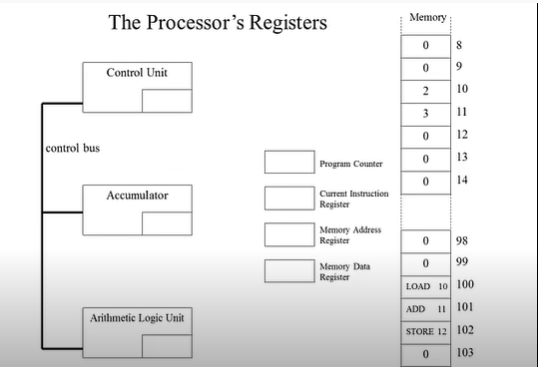
By adding just one new line to the address bus, it doubles the maximum addressable memory.

1. Explain the *Instruction cycle* of the processor by taking an example of the program

Load: [10]

Add: [11]

Store: [12]



The CPU sends the contents of the PC to the MAR and sends a read command on the control bus. In response to the read command (with address equal to PC), the memory returns the data stored at the memory location indicated by the PC on the data bus. The CPU copies the data from the data bus into its MDR. A fraction of a second later, the CPU copies the data from the MDR to the instruction register for instruction decoding. The PC is incremented so that it points to the next instruction. This step prepares the CPU for the next cycle.

1. Write short notes on the following topic:
2. Von Neumann and Harvard Architecture:

**Von Newman** consists of a Control Unit, ALU, Registers and Inputs/Outputs. In this architecture the instruction data and program data are stored in the same memory. By using the same data bus to fetch instruction and data operation, it experiences bottle-neck. Still, Von Neumann architecture is the design upon which many general-purpose computers are based and this design is still used in most computers produced today.

**Harvard architecture** is a computer system which contains two separate areas for commands or instructions and data. This architecture overcomes the bottleneck of Von Neumann Architecture by having two separate buses for instruction and data, due to which the CPU can access instructions and read/write data at the same time making this the the main advantage of this architecture.

1. RISC vs CISC architecture

**Reduced Instruction Set Computer (RISC)** is physically small computer. It processes a limited number of relatively simple instructions. It breaks each instruction down into even simpler instructions which helps it to carry out those instructions quickly. By being small in size it is also uses less circuits. It is mainly used in mobile phones and embedded system.

**Complex Instruction Set Architecture (CISC)** is physically larger computer. It processes more complex instructions as a single instruction will do all loading, evaluating, and storing operations, hence it’s complex. Since it is large in size it also needs more complex circuits which in turn needs more power. It is mainly used in modern computers.